Amendments to the Specification:

Please amend the specification as follows:

Page 6, replace the paragraph beginning on line 26 with the following rewritten paragraph:

In order to previously design and manufacture the ~~common~~ non-customized layer masks for the non-customized layers, the following two conditions must be met. The first condition is as follows: It is necessary to fix patterns for functional elements or devices such as transistors for constituting each non-customized layer and avoid changes in patterns after the design and fabrication of the mask are started. Further, the second condition is as follows: Interconnections in each wiring layer used as a customized layer are suitably formed in association with the non-customized layer so that desired functions are obtained. Namely, if basic gates (also called "basic cells") based on the gate array system are partially embedded in the IC designed by the standard cell system or full custom system, and the plurality of embedded basic gates are electrically connected to one another and utilized in combination so as to implement the desired functions, then the ~~common~~ non-customized layer masks used for the non-customized layers can be designed and fabricated prior to the formation of the customized layer even in the case of the IC designed by the standard cell system or full custom system.

Page 7, replace the paragraph beginning on line 17 with the following rewritten paragraph:

A process for designing such an IC as to allow the ~~common~~ non-customized layer masks for the non-customized layers to be designed and fabricated prior to the formation of the customized layer, using the standard cell system or full custom system will next be explained.

Page 7, replace the paragraph beginning on line 28 with the following rewritten paragraph:

Next, design resources based on the gate array system are blocked to effect layout design on the area having the potential of change in circuit. The layout of the entire IC is designed while the blocked design resources based on the gate array system are being captured by a CAD (Computer Aided Design) of the standard cell system or full custom system. Upon completion of the layout design of the entire IC, the design and fabrication of the ~~common~~ non-customized layer masks related to the non-customized layers is started.

Page 8, replace the paragraph beginning on line 8 with the following rewritten paragraph:

Thereafter, when the contents of the circuit is determined in the area having the potential of the change in circuit, each gate array block corresponding to a basic cell block is again laid out using the CAD of the gate array system. The design and fabrication of a circuit mask corresponding to each customized layer are started based on the re-laid out gate array block. Incidentally, the gate array block whose circuit has been determined, is laid-out in a design based on the non-customized layers formed by the previously-designed and fabricated ~~common~~ non-customized layer masks. Namely, the gate array block preceding the determination of the circuit and the gate array block subsequent to the determination of the circuit are respectively made up of the same basic gate comprised of basic gates identical in number in both the vertical and horizontal directions.

Page 10, replace the paragraph beginning on line 4 with the following rewritten paragraph:

Since diffused layers, polysilicon layers, metal wiring layers, etc. are conventionally formed after the design and fabrication of the masks when the IC is designed by the standard cell system or full custom system, it normally took several months to complete the IC. On the other hand, according to the IC chip 1 in an embodiment of the present invention, it is possible to previously design and manufacture the ~~common~~ non-customized layer masks corresponding to the non-customized layers during a logic-simulation stage, for example. Further, the design work such as the logic simulation or the like is continuously performed in parallel with the design and fabrication of the ~~common~~ non-customized layer masks. Thereafter, when the corresponding circuit for the gate array block 34 has been determined, the layout of the gate array block 34 is designed again, and the circuit mask corresponding to a customized layer is designed fabricated.